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APPLICATION FOR U.S. LETTERS PATENT

Title:

POWER SUPPLY SYSTEM AND METHOD FOR SUPPLYING POWER TO CPU PROVIDING POWER SAVING MODE

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AMPLIFYING CIRCUIT, SPEAKER SYSTEM, AND MOBILE INFORMATION TERMINAL EMPLOYING AMPLIFYING CIRCUIT

[0001] This application claims priority under 35 USC § 119 to Japanese Patent Application No, 2002-289862 filed on October 02, 2002, the entire contents of which are herein incorporated by reference.

[0002] The present specification relates to a power supply system and method for supplying power to a CPU having a power saving mode, and in particular to a power supply system and method for supplying power to a CPU while preventing the CPU from erroneously stopping when operating under a power saving mode.

BACKGROUND OF THE INVENTION

[0003] Many mobile information devices such as laptop personal computers, cellular phones, etc., include a power saving mode for the purpose of saving battery power when the devices are in a standby state.

[0004] Specifically, in a conventional cellular phone, a battery power supply VBAT, utilizing 3.6 volts is transformed by a regulator 5 into a constant voltage Vcc having 2.0 volts, and is supplied to a CPU 2, which in turn is connected to an operation key 3 and a reception section 4 as shown in FIG. 6. In such a conventional configuration, when the operation key 3 is not activated for more than a prescribed time period, the CPU 2 switches an internal circuit to a low voltage operation condition in order to save power.

The CPU 2 simultaneously outputs a voltage switching signal, under a power saving mode, to the regulator 5 so as to decrease a power output from the regulator 5.

[0005] The cellular phone is generally driven by a battery power supply VBAT. When an output of the battery power supply VBAT becomes lower than or equal to 2,0 volts, an output of the regulator 5 also becomes lower than or equal to 2,0 volts. Accordingly, a voltage detecting section is generally provided to continuously output reset signals to the CPU 2 so as to deactivate the CPU 2 in order to avoid operation when the output of the regulator 5 becomes less than or equal to a prescribed reference voltage (e.g., 1.9 volts). However, when the CPU 2 of the cellular phone enters into the power saving mode under the above-mentioned procedure, the voltage detecting section also detects such a decreased voltage and outputs a reset signal to the CPU 2. As a result, the CPU 2 is deactivated.

BRIEF SUMMARY OF THE INVENTION

[0006] Accordingly, an exemplary embodiment of the present invention provides an improved power supply system for supplying power to a CPU that preferably provides a power saving mode to a mobile information device.

[0007] The power supply system under an exemplary embodiment includes a power supplying section that supplies the CPU with a prescribed supply voltage, and a voltage detecting section that outputs a reset signal resetting the CPU when the supply

voltage is equal to, or below a prescribed voltage detection value. Furthermore, a control section operates to decrease the supply voltage to a prescribed power-save level when the power saving mode is set. The control section decreases the supply voltage to be less than or equal to the power save level when the power saving mode is set. The control section also recovers the prescribed voltage detection value (or reset level) after recovering the supply voltage when the power saving mode is terminated.

[0008] In another exemplary embodiment, a power supplying section switches the power supply voltage from a first to a second level that is lower than a first level, using a first switching signal. The power supplying section also changes the first switching signal from a first to a second condition when a power saving mode is set. A voltage detecting section changes the voltage detection value (or reset level) from a fist to a second level, where the second level is lower than the first level, by using a second switching signal. The voltage detection section also changes the second switching signal from a first to a second condition when the power saving mode is set. The control section then changes the second switching signal from a first to a second condition after changing the first switching signal from a first to a second condition.

[0009] In yet another exemplary embodiment, the control section returns the second switching signal to the second level after returning the first switching signal to the fist condition when the power saving mode is terminated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The present disclosure and features and advantages thereof will be more readily apparent from the following detailed description and appended claims when taken with drawings, wherein:

[0011] FIG. 1 illustrates an exemplary cellular phone employing a CPU providing a power saving mode according to a first embodiment;

[0012] FIG. 2 illustrates a power supply control section used in FIG. 1;

[0013] FIG. 3 illustrates exemplary signals and their waveforms output from the power supply control section;

[0014] FIG. 4 illustrates another exemplary cellular phone employing a CPU providing a power saving mode;

[0015] FIG. 5 illustrates a procedure executed by the CPU illustrated in FIG. 4; and

[0016] FIG. 6 illustrates a conventional cellular phone.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Referring now to the drawings, wherein like reference numerals and marks designate identical or corresponding parts throughout several views, in particular in FIG. 1, a cellular phone 1 is described under a first exemplary embodiment. Cellular phone 1includes a power supply control section 100 that adjusts an output of a battery power supply VBAT, a CPU 2, an operational key 3 , and a reception section 4. The CPU 2 provides a power saving mode and outputs a voltage switching signal SI of a low level to the power supply control section 100 during a power saving mode. The CPU 2 also outputs a voltage switching signal SI of a high level to the power supply control section 100 during a normal operation mode.

[0018] The power supply control section 100 includes a regulator 10, a control section 20, and a voltage detecting section 30. Exemplary configurations and operations of these devices are now described.

[0019] The regulator 10 ordinarily outputs a constant voltage Vcc 1 of 2.0 volts by transforming a battery power supply VBAT, having an initial output of 3.6 volts. The regulator 10 also outputs a constant voltage Vcc 2 that is lower than voltage Vcc 1 in response to a low level REG switching signal S2, which is transmitted from the control section 20. Under this configuration, the regulator 10 serves as a power supply section, supplying the CPU 2 with power in collaboration with the battery power supply VBAT.

[0020] The voltage detecting section 30 outputs a reset signal S4 to the CPU 2 when an output voltage Vcc (e.g. Vccl or Vcc2) output by the regulator 10 becomes less than a later mentioned prescribed voltage detection value, set in the voltage detecting section 30. A prescribed voltage detection value may be derived from (Vref x ((r4 + r5)/r5)) or (Vref x ((r4 + r5 + r6)/(r5 + r6))).

[0021] The control section 20 decreases the prescribed voltage detection value from the first to second level in response to a low level voltage switching signal SI when a power saving mode is set (i.e., when Vcc2 is larger than the second level, and the first level is larger than the Vcc2). The first and second levels correspond to the voltage reference detection values (Vref x ((r4 + r5 + r6)/(r5 + r6))) and (Vref x ((r4 + r5)/(r5))),

respectively. Subsequently, the control section 20 decreases voltage Vcc, output from the regulator 10, down to Vcc2 from Vccl. Further, when the low level voltage switching signal SI is stopped for the purpose of terminating the power saving mode, the control section 20 synchronously controls the regulator 10 to recover the output voltage Vccl, and after that controls the voltage detecting section 30 to recover the first voltage level.

[0022] The regulator 10, control section 20, and voltage detecting section 30 are now described in more detail with reference to FIG. 2.

[0023] The regulator 10 of FIG. 2 outputs a constant voltage Vccl of 2.0 volts from the battery power supply VBAT, and has an initial output value of 3 . 6 volts as mentioned above. The regulator 10 includes a P-channel type MOSFET 12 generating an output based upon the output from the battery power supply VBAT in accordance with a voltage applied to its gate terminal as a control signal from comparator 11. A reference voltage "Vref" generated by a regulator (not shown) is input to a positive input terminal of the comparator 11. A signal obtained by dividing an output of the MOSFET 12 with a resistance division circuit formed from resistances rl to r3 is input to a negative input terminal of the comparator 11. A switch SW1 is turned OFF by an input of an REG switching signal S2 (a first switching signal) of a high level.

[0024] The voltage detecting section 30 includes comparator 31. A value obtained by dividing Vccl of 2.0 volts of the regulator 10 with a resistance division circuit formed from resistances r4 to r6. The value is then applied to a positive input terminal of the comparator 31. A reference voltage Vref generated by a regulator (not shown) is input to the negative input terminal of comparator 31. Switch SW2 is turned OFF by a high-level input of a VDET switching signal S3 (a second switching signal).

[0025] The control section 20 includes a plurality of signal generating circuits Cl and C2, each of which respectively generate a REG switching signal S2 and a VDET switching signal S3. Signal generating circuits C1 and C2 each branch off from an inverter 21 to which a voltage switching signal SI is input from the CPU 2. The voltage switching signal SI is input to the signal generation circuits Cl and C2 via the inverter 21.

[0026] The signal generation circuit Cl includes three inverters 22 to 24, which are serially connected as shown in FIG. 2. A condenser 24 is disposed between the inverters 23 and 25, and is grounded at one end. The signal generation circuit C2 includes a CMOS inverter 26, driven by a constant current source 27, a condenser 28, and a buffer circuit 29.

[0027] Respective waveforms of the voltage switching signal SI output from the CPU 2 to the control section 20, a voltage VA appearing at a position "A" in the signal

generation circuit Cl, the REG switching signal S2, a voltage VB appearing at a position "B" in the signal generation circuit C2, the VDET switching signal S3 , and a reset signal S4 output from the voltage detecting section 30 are described with reference to the control section 20 and FIGS. 2 and 3.

[0028] The condenser 24 preferably has a larger capacity than the condenser 28 , so that the voltage VA can more gently decrease than the voltage VB at a time of a falling edge of the voltage switching signal SI. By employing such a configuration, the VDET switching signal S3 initially drops to a low level on a falling edge as shown in FIG. 3. After a period of time tl has elapsed, the REG switching signal S2 also falls down as illustrated in FIG. 3.

[0029] Further, the voltage appearing at the position "A" (FIG. 2) rises up at a time of a rising edge of the voltage switching signal SI at the same speed at which it drops. At the position "B" (FIG. 2), however, the voltage gently rises up due to a function of the constant current source 27. Accordingly, the REG switching signal S2 initially rises up when the voltage switching signal SI rises up. Then, when a time t2 has elapsed, the VDET switching signal S3 rises up as illustrated in FIG. 3.

[0030] By employing such a configuration, an erroneous output of a reset signal (e.g. ON) to the CPU 2 can be avoided. The erroneous reset signal is typically generated when either the constant voltage output Vcc descends from Vccl to Vcc2 (that is lower

than Vrefl) before a voltage detection value defined by the voltage detection section 30 descends to the second level (i.e., v2=Vref x (r5)/(r4 +r5)) from the first level (i.e., v1 = Vref x (r4 + r5)/(r4 + r5 + r6)), or when the voltage detection value recovers the first level from the second level before the constant voltage Vcc recovers the output voltage Vccl from the Vcc2.

[0031] A second embodiment is now described with reference to FIG. 4. As shown, the illustrated embodiment includes a power supply control section 200 that emulates the power supply control section 100 of the first embodiment by partially utilizing a function of the CPU 2.

[0032] Specifically, a regulator 210 includes a P-channel type MOSFET 213 that adjusts its output in accordance with a voltage applied to its gate as a control signal in the similar manner as performed by the regulator 10 of the first embodiment. Regulator 210 includes a comparator 212 that outputs electric signals to the gate of the MOSFET 213. A reference voltage Vref provided by a regulator (not shown) is applied to a positive input terminal of the comparator 212. A D/A converter 211 is connected to a negative input terminal of a comparator 212 so as to output analog signals Vccl from 2.0 to 0 volts, based upon the output from the FET 213 in accordance with digital signals 0 to 256. The CPU 2 outputs an REG setting signal (a first switching signal) of 127 values

(decimal expression) to the D/A converter 211 when an operation mode runs with the ordinary voltage.

[0033] A voltage detecting section 250 includes a D/A converter 251 that outputs analog signals Vccl from 2.0 to 0 volts based upon the output from the FET 213 in accordance with digital signals of from 0 to 256. A comparator 252 receives analog signals from the D/A converter 251 at its positive input terminal, and receives an input of a reference voltage vref generated by a regulator (not shown) at its negative input terminal. An output of the comparator 252 serves as a reset signal S4 for resetting the CPU 2. When an operation mode runs with normal operating voltage, the CPU 2 outputs a VDET setting signal (a second switching signal) of 130 values to the D/A converter 251.

[0034] An operation of the second embodiment, which is controlled by the CPU 2, is now described with reference to FIG. 5. First, a timer is initiated in step S1. When none of key inputs and signal receptions exists ("No", in steps S2 and S3) and the timer times out ("Yes", in step S4), the VDET switching signal is changed from 130 down to 50 values so that a voltage detection value set in the voltage detecting section 250 decreases in order to prevent the detecting section 250 from outputting a reset signal S4 to the CPU 2 (step S5). Then, the REG setting signal is changed from 127 down to 48 values, so that the output value Vcc of the regulator 210 is decreased (step S6).

[0035] When the CPU 2 detects any one of the key inputs and signal receptions ("Yes", in steps S2 or S3) , the CPU 2, operating in the power saving mode, initially returns the value of the REG setting signal from 48 up to 127 values, and thereby recovers the output voltage Vcc and the normal operation mode (step S7). The CPU 2 then changes the VDET setting signal from 50 back to 130 values in order to prevent the voltage detecting section 250 from outputting the reset signal S4 to the CPU 2 (step S8). Since such recoveries are performed only by changing values of REG and VDET setting signals, it is not a particular burden on the CPU 2, and can be employed even during the power saving mode. After that, the process returns to step S1 to start the timer again.

[0036] Numerous additional modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the present invention may be practiced otherwise than as specifically described herein.